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CSE-45208
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Lab #3

Dr. Izadi

Using D flip-flops (7474) and available gates in the lab, you need to design a circuit to generate the following sequence as specified below.

$$\begin{array}{c} \downarrow 1 \rightarrow 5 \rightarrow 2 \rightarrow 4 \rightarrow \\ \leftarrow & X = 0 \end{array} \qquad \qquad \qquad \leftarrow 1 \leftarrow 5 \leftarrow 2 \leftarrow 4 \leftarrow \\ X = 1 \end{array}$$

Your report should include a detailed documentation of the following two designs:

- a. In this design, the sequence counts should be assigned to the states.
- b. In the second design, the sequence counts should be assigned to the output of the sequential circuit.

You should implement both designs using Electronic Workbench and verify their operations. Furthermore, you need to implement one of your designs (your choice) on a breadboard, verify its operation and have it signed off by the instructor or your TA.

For a tutorial on sequential design click here.